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| Deu_logo | **DOKUZ EYLUL UNIVERSITY**  **ENGINEERING FACULTY**  **DEPARTMENT OF COMPUTER ENGINEERING** | logo-en |

**CME1214 LOGIC DESIGN**

**PRELIMINARY REPORT**

**LAB 3**

**by**

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**Lecturers**

**Instructor Dr. Özlem Öztürk**

**Res.Asst. Dr. Feriştah Dalkılıç**

**Res.Asst. Özlem Yerlikaya**

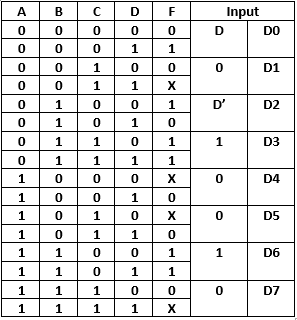
**Res.Asst. Gökmen Katipoğlu**

**IZMIR**

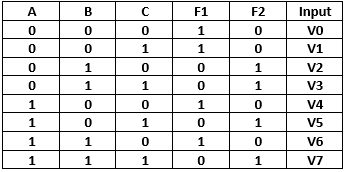
**09.04.2019**

* + - 1. **TRUTH TABLE**

**1.Experiment**

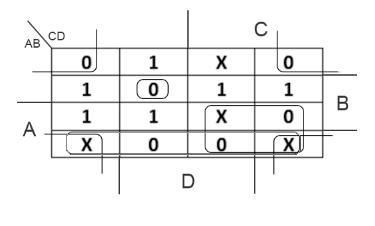


**2.Experiment**



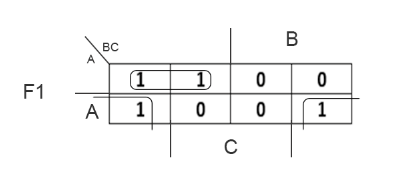
* + - 1. **KARNAUGH MAPS**

**1.Experiment**

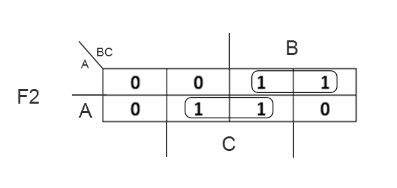


**F** = (B+D) \* (A’+B) \* (A’+C’) \* (A+B’+C+D’)

**2.Experiment**



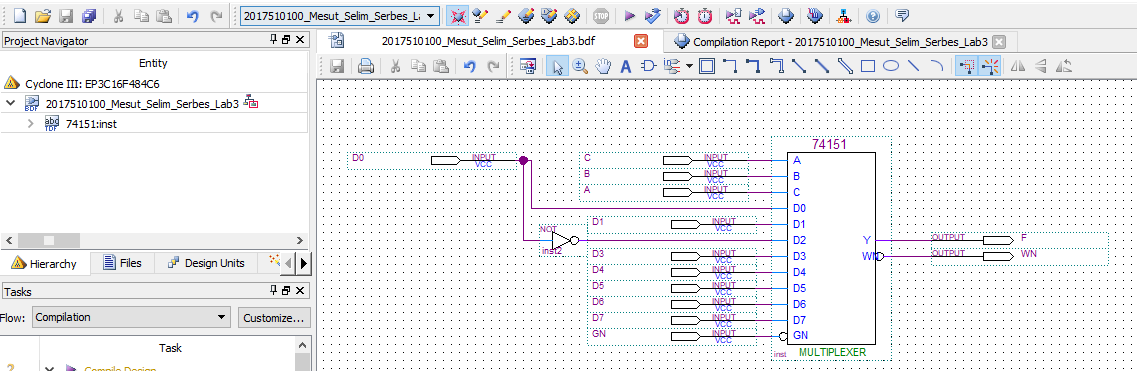
**F1** = (A’\*B’) + (A\*C’)



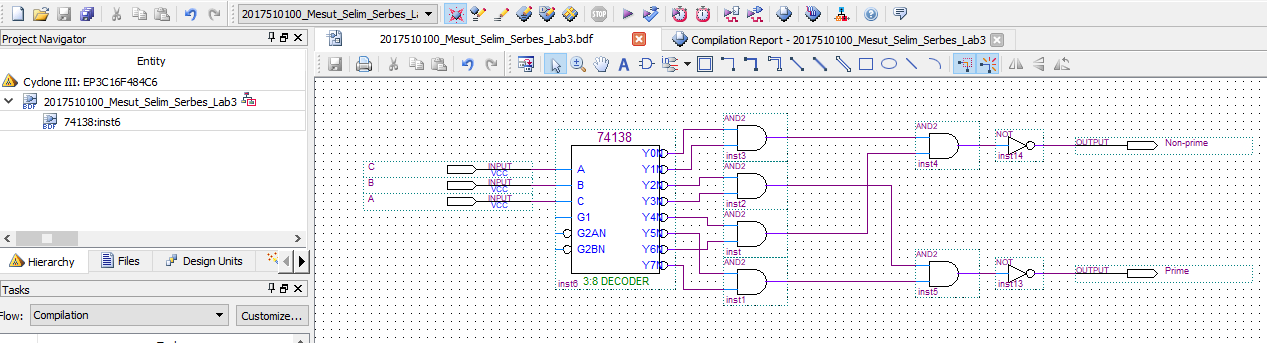
**F2** = (A’\*B) + (A\*C)

* + - 1. **LOGIC DIAGRAM**

**1.Experiment**



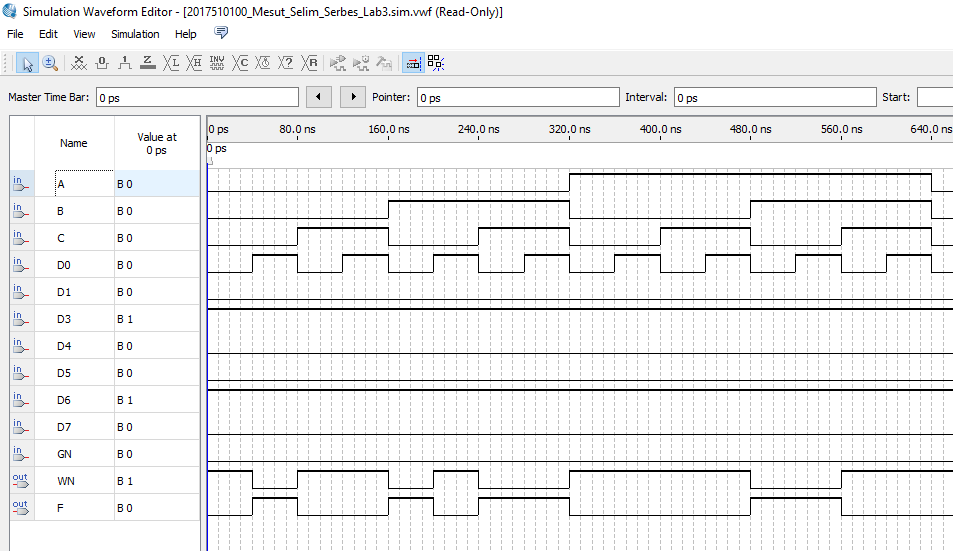
**2.Experiment**



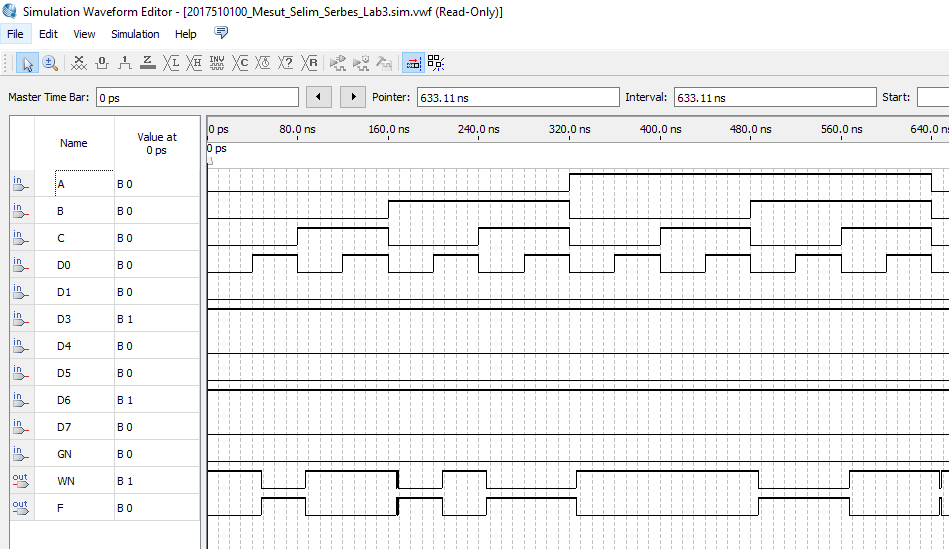
* + - 1. **WAVEFORMS**

**1.Experiment**

**Functional Waveform**

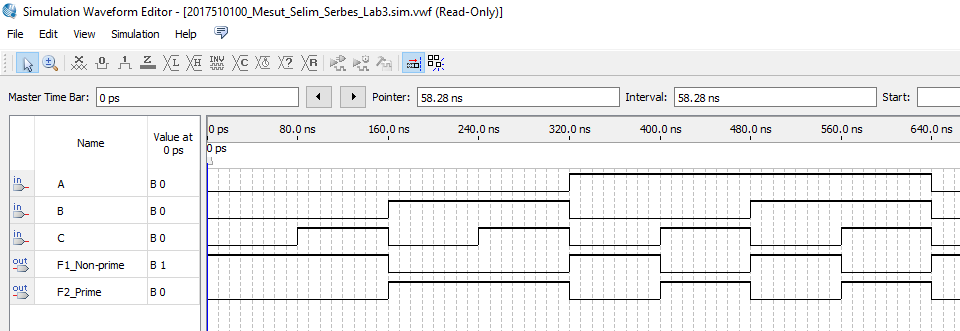
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**Timing Waveform**

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**2.Experiment**

**Functional Waveform**

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**Timing Waveform**

